REMARKS

Reconsideration and allowance of this application, as amended, is respectfully requested.

This amendment is in response to the Office Action dated September 4, 2003. By the present amendment, the original independent claims 1 and 3 have been replaced by new independent claims 17 and 19. In addition, new dependent claims 18 and 20 have been added, and claim 2 has been amended to change its dependency to newly presented independent claim 17. Also, the nonelected claims 9-16 have been cancelled, without prejudice to the Applicants' right to proceed with filing a Divisional application directed to these nonelected claims.

Briefly, the present invention is directed to an improved semiconductor integrated circuit module that reduces wiring for the power supply path and suppresses unnecessary radiation of electromagnetic noise (e.g. see page 5 and 6 of the specification). Referring to Fig. 12, a comparison can be seen between an embodiment of the present invention (shown on the right side of Fig. 12) and a conventional structure (shown on the left side of Fig. 12). As discussed on page 5 of the specification, in the embodiment of the present invention shown on the right side of Fig. 12, it can be seen that a power supply module 11 is located above LSI package 13 which includes a semiconductor chip 19. On the other hand, in the conventional structure shown in the left side of Fig. 12, the power supply module 11 is located at a separate position on the substrate 16 away from the LSI package 13 and the chip 19. As discussed in the last paragraph on page 5 and the third paragraph on page 6 of the specification, the advantage of the arrangement of the present invention shown in the right hand side of Fig. 12 is a shortened power supply

path from the power supply module 11 to the LSI chip 13. In addition, the power supply module is close to the shielding surface of the LSI package 13, thereby suppressing unnecessary radiation of electromagnetic noise.

Figs. 1 and 2 show details of a first embodiment of a semiconductor integrated circuit module with the power supply module 11 located above the LSI package. As discussed on pages 7 and 8, two different wiring paths exist for supplying power to the semiconductor chip 19 in this arrangement. The first path provides power to the LSI chip from the substrate 16 (shown, for example, in Fig. 12). This first path extends through the solder ball 181, the throughhole 301, the electrode 121 and the wires 153 and 154 to supply power from the substrate to the chip 19. In addition, a second path for supplying power to the chip 19 from the power supply module 11 is provided. The second path goes through the electrode 122, the throughhole 302 and the bonding wire 156. By virtue of these two separate paths, in conjunction with the location of the power supply module 11 on an upper surface of the LSI package, the power supply wiring can be significantly shortened and unnecessary electromagnetic radiation can be suppressed.

Reconsideration and allowance of newly submitted claims 17 and 19 and their dependent claims over the cited prior art to Jeon (USP 6,432,750), Masanobu (JP 8279593), Chen (USP 6,394,175) and Lin (USP 6,184,580) is respectfully requested. By the present amendment, new independent claims 17 and 19 both define the location of a power supply module on an upper surface of the semiconductor package. These claims also define the two separate power supply paths for providing power to a semiconductor integrated circuit with the LSI package. For example, referring to claim 17, the first path from the substrate to the IC chip is set

forth through the plurality of first bonding wires (e.g. 153/154), a solder ball (e.g. 181) connecting the semiconductor package to a substrate, a first conductive throughhole (e.g. 301) and a first electrode (e.g. 121). A second power supply path is also defined from the power supply module to the IC chip via a second electrode (e.g. 122), a second conductive throughhole (e.g. 302) and a second bonding wire (e.g. 156). Incidentally, it is noted that the references to the numerals used in Figs. 1 and 2 are solely for purposes of example, and not intended to limit the specifics of these claims.

Although the various references to Jeon, Masanobu, Chen and Lin are all of general interest regarding supplying power to an IC chip, it is respectfully submitted that none of them teach of suggest the combination of features set forth in independent claims 17 and 19 and their dependent claims. In particular, none of these references, whether considered alone or in combination, teach the claimed location of the power supply module on an upper surface of a semiconductor package and the two separate power supply paths, one from the substrate and one from the power supply module, set forth in detail in the structural limitations of independent claims 17 and 19. Therefore, reconsideration and allowance of new independent claims 17 and 19, and the dependent claims 2, 4-8, 18 and 20 over these references is earnestly solicited.

Request for Telephone Interview:

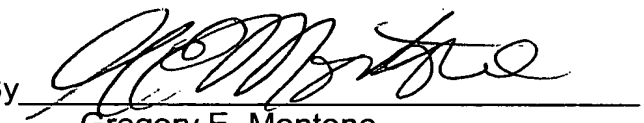
If, after the Examiner has studied the proposed amendments and the above comments, it is determined that this application is not in condition for allowance, it is requested that the Examiner contact the undersigned attorney for purposes of

conducting a telephone interview to discuss this application and the amended claims. Alternatively, if the Examiner would prefer to conduct a person interview in this matter, it is requested that the Examiner contact the undersigned attorney so that arrangements can be made for such a personal interview. Applicants and the undersigned attorney greatly appreciate the Examiner's cooperation and courtesy in this regard.

To the extent necessary, Applicants petition for an extension of time under 37 CFR 1.136. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to the Antonelli, Terry, Stout & Kraus, LLP Deposit Account No. 01-2135 (Docket No. 501.41215X00), and please credit any excess fees to such Deposit Account.

Respectfully submitted,

ANTONELLI, TERRY, STOUT & KRAUS, LLP

By 

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APPENDIX I

ABSTRACT OF THE DISCLOSURE

In the past, a power supply distance between a power source and an LSI package could not be shortened and power supply variations could easily produce an adverse effect. To reduce the power supply distance between the LSI and power supply module the power supply module is mounted on an upper surface of the LSI package. As a result, the power source noise can be reduced, the efficiency and response rate of the power source unit are high, and the generated electromagnetic field can be reduced. Moreover, since each LSI package has a power supply module required therefor, the number of required power source types (voltage types) on the substrate with the package mounted thereon can be decreased. As a result, the mounting efficiency can be increased and the substrate can be manufactured at a low cost.